इग्नू जन-जन का विश्वविद्यालय

इन्दीरा गांधी राष्ट्रीय मुक्त विश्वविधालय
INDIRA GANDHI NATIONL OPEN UNIVERSITY
क्षेत्रीय केन्द -राजकोट. REGIONAL CENTRE - RAJKOT

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Assessment Sheet

Enrolment No. 156847878 Programme BCA Assessment

Student's Name ABC Course MCS-012 Grade/Marks

Study Centre Code No. 42012 Assignment No. 01 Max. Marks

Evaluator's Comments

(If this space is not sufficient, please use back page)

Please tick ✔ in the relevant box below

CONTENT			STRUCTURE & PRESENTATION		
Accurate Informaton	☐☐☐☐☐☐	Inaccurate Information	Well Planned	☐☐☐☐☐☐	Inadequately Planned
Adequate Coverage Good	☐☐☐☐☐☐	Inadequate Coverage Poor	Concise	☐☐☐☐☐☐	Too long or too short
Coneeptual Analysis Good	☐☐☐☐☐☐	Conceptual Analysis Poor	Clearly Expressed	☐☐☐☐☐☐	Not Clearly Expressed

Evaluator's Signature

Date

Name in full

Evaluator's Code No.

Address

Moderator's Comments, if any

Signature of the Moderator

Name in full

BACHELOR OF COMPUTER APPLICATIONS (BCA)

(Revised Syllabus)

BCA(Revised Syllabus)/ASSIGN/SEMESTER-II

ASSIGNMENTS

(July - 2019 & January - 2020)

MCS-011, MCS-012, MCS-015, MCS-013, BCSL-021, BCSL-022,

SCHOOL OF COMPUTER AND INFORMATION SCIENCES
INDIRA GANDHI NATIONAL OPEN UNIVERSITY
MAIDAN GARHI, NEW DELHI – 110 068

Course Code	**:**	**MCS-012**
Course Title	**:**	**Computer Organisation and Assembly Language Programming**
Assignment Number	**:**	**MCA(2)/012/Assignment/2019-20**
Maximum Marks	**:**	**100**
Weightage	**:**	**25%**
Last Dates for Submission	**:**	**15th October, 2019 (For July 2019 Session)** **15th April, 2020 (For January 2020 Session)**

There are four questions in this assignment, which carries 80 marks. Rest 20 marks are for viva voce. You may use illustrations and diagrams to enhance the explanations. Please go through the guidelines regarding assignments given in the Programme Guide for the format of presentation. Answer to each part of the question should be confined to about 300 words. Make suitable assumption, if any.

Q1. (Covers Block 1)

(a) Please refer to Figure 4 of Unit 1 of Block 1 on page 11. Assuming the same machine to be used for execution of the following three consecutive instructions:

LOAD C ; Loads the content of Memory location C into the Accumulator Register.

ADD B ; Adds the content of memory location B in the Accumulator Register.

STORE A ; Stores the content of Accumulator register AC in memory location A.

The following are the details about the instructions, data and registers:

- Each word of memory is of 32 bits in length. Each instruction is also 32 bits long.
- Main Memory has 256 words.
- The three consecutive instructions as shown above starts from memory location $(1F)_h$; A is at location $(FD)_h$ and contains a value $(1000)_h$, B is at location $(FE)_h$ and contains a value $(FF3B)_h$ and C is at location $(FF)_h$ and contains a value $(2A2F)_h$.
- The AC, IR and MBR registers are of size 32 bits, whereas PC and MAR registers are of size 8 bits. The initial content of PC register is (1F)h

Draw the diagrams showing addresses and content of memory locations and Registers. Show how the content of memory locations and registers will change with the execution of the three instructions. Show all the addresses and values in hexadecimal notations. You must also perform the necessary arithmetic using signed 2's complement notation and show the results indicating overflow, if any. Also explain the process of execution of the instructions. **(4)**

(b) Perform the following conversion of numbers: **(2)**

i) Decimal $(3412454512)_{10}$ to binary and hexadecimal
ii) Hexadecimal $(FEDCBA9)_h$ into Octal.
iii) String "In file name % means blank." into UTF 8
iv) Octal $(7766432)_o$ into Decimal

(c) Assuming that inverse is represented as ', simplify the following Boolean functions:
F= ((A' + B)' + (A'+B')')' **(1)**

(d) Simplify the following function using K-map: F(A, B, C, D) = Σ (0, 2, 6, 8, 10, 14)
Draw the circuit using NAND gates. **(2)**

(e) Consider the Adder-Subtractor circuit as shown in Figure 3.15 page 76 of Block 1. Explain how this circuit will perform subtraction, if the value of A is 1111 and B is 1100. You must list all the bit values including Cin and Cout and overflow condition. **(1)**

(f) Explain the functioning of a 2× 1 Multiplexer. You must draw its truth table and explain its logic diagram with the help of an example input. **(2)**

(g) Assume that a data value 1111 was received as 1011. Explain how use of Hamming's Error-Correcting code will send this data value from source and correct error at the destination. **(2)**

(h) Explain functioning of S-R flip flop with the help of logic diagram, characteristic table and excitation table. **(2)**

(i) Explain the functioning of Asynchronous and Synchronous counter. Explain how they are different from each other. **(2)**

(j) Differentiate between fixed point numbers and floating point numbers? Explain the representation for Zero in IEEE 754 single precision standard. Represent $(-32.25)_{10}$ and $(0.000125)_{10}$ in IEEE 754 single precision format. **(2)**

Q2. (Covers Block 2)

(a) Reference Figure 2(b) on page 8 in Unit 1 of Block 2. Draw the Internal organisation of a 64×8 RAM. Also answer the following:
(i) How many data input and data output lines does this RAM needs? Explain your answer.
(ii)How many address lines are needed for this RAM? Give reason in support of your answer.
(2)

(b) A computer has 16 MB RAM and has a word size of 32 bits. It has cache memory having 16 blocks having a block size of 64 bits. Show how the main memory address $(17F0AB)_h$ will be mapped to cache address, if

(i) Direct cache mapping is used
(ii) Associative cache mapping is used
(iii)Two way set associative cache mapping is used.
You must clearly identify tag, index, main memory block address and offset etc. in your answer. **(3)**

(c) Explain the process of Interrupt handling and Return from interrupt with the help of a diagram. You must answer this question in your own words. **(2)**

QUESTION

AND

YOUR HAND WRITTEN

ANSWER